Customer No.: 31561
Application No.: 10/064,916
Docket No.: 7558-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original)A multi-memory architecture with an externally accessible storage capacity known as a total memory capacity and the number of pins of the multi-memory architecture having the total memory capacity is known as a total pin number, wherein the total pin number comprises used and unused pins, the multi-memory architecture comprising: a first memory device having a first data storage capacity and a first predefined pin configuration having a first number of pins which is the actual number of used pins according to the first data storage capacity; and

a second memory device having a second data storage capacity and a second predefined pin configuration having a second number of pins which is the actual number of pins according to the second data storage capacity; wherein the first number of pins is greater than the second number of pins, and the total number of pins of the multi-memory architecture is not less than the number of pins of the first memory device of multi-memory architecture having the total memory capacity.

2. (original)The multi-memory architecture of claim 1, wherein the externally-accessible total data storage capacity of the multi-memory architecture is equal to the data storage capacity of the first memory device plus the data storage capacity of the second memory device.

3. (original) The multi-memory architecture of claim 1, wherein the second memory device comprises a plurality of segments and each segment has a data storage capacity equal to the data storage capacity of the first memory device; wherein the storage space of the first memory device is used to replace one of the segments in the second memory device so that an access to the replaced segment is mapped to the storage space of the first memory device.

4. (original) The multi-memory architecture of claim 3, wherein the segment in the second memory device that is currently being replaced by the first memory device is used to replace any one of the segments in the second memory device other than the one currently being replaced by the first memory device.

5. (original) The multi-memory architecture of claim 3, further comprising: at least one replacement segment in the second memory device, whose data storage capacity equals to each segment in the second memory device is used to replace any one of the segments in the second memory device other than the one being currently replaced by the first memory device.

6. (original) The multi-memory architecture of claim 1, further comprising a replacement memory area, whose data storage capacity equals to the second memory device, which is partitioned into a plurality of segments each being equal in data storage capacity to the first memory device; the replacement memory area is used to replace the

second memory device to allow the externally-accessible total storage space of the multi-memory architecture to cover the currently-accessed memory device selected from the second memory device, the replacement memory area excluding the storage space of the segment currently being replaced by the first memory device, and the first memory device in some segments of the currently-accessed memory.

7. (original) The multi-memory architecture of claim 6, wherein the segment currently being replaced by the first segment is replaced by any one of the segments in the currently-accessed memory device other than the one being currently replaced by the first memory device.

8. (original) The multi-memory architecture of claim 6, wherein the second memory device further comprising a plurality of second memory replacement segments, each being equal in data storage capacity to each segment in the currently-accessed memory device, which is used to replace any one of the segments in the currently-accessed memory device other than the segment currently being replaced by the first memory device.

9. (original) The multi-memory architecture of claim 1, wherein the pin configuration of the first memory device having a total data capacity which is the sum of the first and second data capacities.

10. (original) A multi-memory architecture comprising:

a first memory device having a first data storage capacity; and

a second memory device having a second data storage capacity;

wherein

an overall pin configuration of the multi-memory architecture is compatible with the pin configuration of the first memory device having the second data storage capacity.

11. (original) The multi-memory architecture of claim 10, wherein the externally-accessible total data storage capacity of the multi-memory architecture is equal to the data storage capacity of the first memory device plus the data storage capacity of the second memory device.

12. (original) The multi-memory architecture of claim 10, wherein the second memory device includes a plurality of segments and each segment comprises a data storage capacity equal to the data storage capacity of the first memory device; wherein the storage space of the first memory device is used to replace one of the segments in the second memory device so that an access to the replaced segment is mapped to the storage space of the first memory device.

13. (original) The multi-memory architecture of claim 12, wherein the segment in the second memory device that is currently being replaced by the first memory device is used to replace any one of the segments in the second memory device other than the one

currently being replaced by the first memory device.

14. (original) The multi-memory architecture of claim 12, further comprising: at least one replacement segment in the second memory device, whose data storage capacity equals to each segment in the second memory device, which can be used to replace any one of the segments in the second memory device other than the one being currently replaced by the first memory device.

15. (original) The multi-memory architecture of claim 10, further comprising a replacement memory area, whose data storage capacity equals to the second memory device, which is partitioned into a plurality of segments each being equal in data storage capacity to the first memory device; the replacement memory area is used to replace the second memory device to allow the externally-accessible total storage space of the multi-memory architecture to cover the currently-accessed memory device selected from the second memory device and the replacement memory area excluding the storage space of the segment currently being replaced by the first memory device, and the first memory device in some segments of the currently-accessed memory.

16. (original) The multi-memory architecture of claim 15, wherein the segment currently being replaced by the first segment is replaced by any one of the segments in the currently-accessed memory device other than the segment being currently replaced by the first memory device.

17. (original) The multi-memory architecture of claim 15, wherein the second memory device further includes a plurality of second memory replacement segments, each being equal in data storage capacity to each segment in the currently-accessed memory device, which is used to replace any one of the segments in the currently-accessed memory device other than the segment currently being replaced by the first memory device.

18. (original) The multi-memory architecture of claim 10, wherein the pin configuration of the first memory device having a total data capacity which is the sum of the first and second data capacities.

19.-26. (canceled)